UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/883,990	06/20/2001	Eiji Koyama	0020-4878P	5654

2292 7590 07/15/2005

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
VILLECCO, JOHN M	

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 07/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/883,990	KOYAMA, EIJI	
	Examiner	Art Unit	
	John M. Villecco	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☒ Claim(s) *5 and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection. More specifically, applicant has added the limitation of the noise component being measured during a manufacturing stage to independent claim 1, thus necessitating the new grounds of rejection presented on the following pages.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hosoya et al. (Japanese Publ. No. 06-283999 A) in view of Hirt et al. (U.S. Patent No. 5,883,830)**.

5. Regarding ***claim 1***, Hosoya discloses a semiconductor integrated circuit for reducing the noise between an analog circuit and a digital circuit. More specifically, Hosoya discloses an analog circuit (14) operating in response to a first clock (CLK2), a digital circuit (12) operating

in response to a second clock (CLK1), a plurality of phase shift circuits (D1-D4) for shifting the phase of the second clock signal (CLK1) from the phase of the first clock signal (CLK2) by a different value, and a spectrum analyzer (30) for measuring the noise generated by the analog circuit (14). See paragraphs 0028-0029 and 0043. Also see Figures 1 and 2. Please see the official translation of the Hosoya reference provided with this action.

Hosoya, however, fails to disclose that the noise component is measuring during a manufacturing stage. It appears that in Hosoya the measurement of the noise only occurs during a prototype (or experimental) stage. Hirt, on the other hand, discloses that it is well known in the art that various variations in process or manufacturing process can cause significant noise within an image sensor. Furthermore, Hirt discloses that by performing compensation on each imager during the manufacturing stage the noise due to process or manufacturing variations can be eliminated. See the abstract and column 5, lines 43-45 and column 1, lines 35-50. Therefore, as taught by Hirt, since process and manufacturing variations produced during the manufacturing process are common, one of ordinary skill in the art would have found it obvious to perform correction on each image sensor produced during the manufacturing process of Hosoya, so that process and manufacturing variations produced during the manufacturing process are eliminated, thus forming a high quality image for every image sensor.

6. As for ***claim 2***, Hosoya discloses that based on code signals, X1-Xk, one of the delay circuits (D1-D4) is selected and noise is measured. A noise is determined for each of the delay circuits and the delay circuit with the least noise is selected and set. See paragraph 0044 and 0050.

7. With regard to ***claim 3***, as mentioned above in the discussion of claim 2, Hosoya discloses all of the limitations of the parent claim. Additionally, Hosoya discloses a minimum of four phase shift circuits. However, Hosoya fails to specifically disclose that noise measuring circuit measures the noise k times. Nevertheless, in order to determine the phase shift circuit, which produces the least amount of noise, each of the phase shift circuits would have to selected and measured. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the noise measuring operation k times (once for each delay element) so that a noise signal can be generated for each of the delay circuits and an optimal delay circuit can be selected.

8. **Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hosoya et al. (Japanese Publ. No. 06-283999 A) in view of Hirt et al. (U.S. Patent No. 5,883,830) and further in view of New, Jr. et al. (U.S. Publ. No. 2001/0047127)**.

9. Regarding ***claim 4***, as mentioned above in the discussion of claim 2, Hosoya discloses all of the limitations of the parent claim. However, Hosoya fails to specifically disclose an operation start control means for starting the selection control means when a specified time has elapsed after having powered on. New, on the other hand, discloses that it is well known in the art to wait a specified time after power up. By waiting for a predetermined time the power supply and clock are allowed to settle. See paragraph 0071. By waiting for the power supply and clock to settle, it is interpreted that the noise from the power supply and the clock settle. By waiting for the noise to settle one can obtain accurate readings of the noise. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to wait

for the power supply and clock have settle for a predetermined amount of time after power up so that accurate noise reading can be made by the noise measuring circuit of Hosoya.

Allowable Subject Matter

10. Claims 5 and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

Regarding ***claim 5***, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest a time measuring means for measuring a second time after termination of successive selection of the phase shift circuits by the selection control means, and operating the selection control means when the second specified time elapses.

As for ***claim 6***, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest that the noise component measured by the noise circuit is a noise component superimposed on a video signal of a shielded region outputted from the image sensing array during one horizontal period and that successive selection of the phase shift circuits by the selection control means is performed in synchronization with a vertical period.

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M. Villecco whose telephone number is (571) 272-7319. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on (571) 272-7308. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).